

CLAIMS

What is claimed is:

- 1 1. A novel architecture for set associative cache, comprising:
2 a set associative cache having a plurality of ways wherein the ways are segmented into a
3 plurality of banks and wherein a first way has a fast access time;
4 access control logic which manages access to the cache and is coupled to said plurality of
5 ways;
6 a plurality of muxes coupled to said first way in each of said banks and coupled to said
7 access control logic; and
8 wherein the access control logic controls the mux in a bank to remap any defective way in a
9 bank to the first way in that same bank.
- 1 2. The architecture of claim 1 wherein said first way has a faster access time because it has a
2 physically shorter path to said access control logic.
- 1 3. The architecture of claim 1 further comprising self test logic coupled to said access control
2 logic to test the cache for defects.
- 1 4. The architecture of claim 3 wherein said self test logic tests the cache for defects on power
2 up.
- 1 5. The architecture of claim 3 wherein said self test logic stores the location of defects in a
2 status register.

1 6. The architecture of claim 5 wherein said access control logic reads the location of defects
2 in the cache from the status register to determine proper control of said muxes.

1 7. The architecture of claim 1 wherein said set associative cache has a data array having a
2 plurality of ways wherein the ways are segmented into a plurality of banks and wherein a first way
3 has a faster access time.

1 8. The architecture of claim 1 comprising a plurality of ways having a fast access time and a
2 plurality of muxes coupled to said plurality of ways in each of said banks and coupled to said
3 access control logic.

1 9. The architecture of claim 8 wherein the access control logic controls the plurality of muxes
2 in a bank to remap any defective way in a bank to a different way in that same bank.

1 10. The architecture of claim 1 wherein the access time of said first way (t_1) is sufficiently fast
2 such that the added time of the mux (t_{mux}) will not add any latency.

1 11. The architecture of claim 10 wherein the access time of said first way (t_1) added to the time
2 of the mux (t_{mux}) is less than or equal to the access time of the slowest way (t_n).

1 12. The architecture of claim 10 wherein the access time of said first way (t_1) added to the time
2 of the mux (t_{mux}) is less than or equal to a system clock cycle (t_{clk}).

1 13. A microprocessor die, comprising:
2 self test logic which tests the die for defects;
3 a set associative cache having a plurality of ways wherein the ways are segmented into a
4 plurality of banks;
5 access control logic which manages access to the cache coupled to said self test logic and
6 coupled to said plurality of ways in said cache;
7 a first way in said cache which has a physically shorter path to said access control logic;
8 a plurality of muxes coupled to said first way in each of said plurality of banks and coupled
9 to said access control logic; and
10 wherein the access control logic controls the mux in a bank to remap any defective way in a
11 bank to the first way in that same bank.

1 14. The microprocessor die of claim 13 comprising a plurality of ways having a physically
2 shorter path to said access control logic and a plurality of muxes coupled to said plurality of ways
3 in each of said banks and coupled to said access control logic.

1 15. The microprocessor die of claim 14 wherein the access control logic controls the plurality
2 of muxes in a bank to remap any defective way in a bank to a different way in that same bank.

1 16. The microprocessor die of claim 13 wherein the access time of said first way (t_1) is
2 sufficiently fast such that the added time of the mux (t_{mux}) will not add any latency to the
3 microprocessor.

1 17. The microprocessor die of claim 13 wherein the access time of said first way (t_1) added to
2 the time of the mux (t_{mux}) is less than or equal to the access time of the slowest way (t_n).

1 18. The microprocessor die of claim 13 wherein the access time of said first way (t_1) added to
2 the time of the mux (t_{mux}) is less than or equal to a system clock cycle (t_{clk}).

1 19. A method of absorbing defects in a set associative cache, comprising:
2 providing a set associative cache with a plurality of ways wherein the ways are segmented
3 into a plurality of banks and wherein a first way has a fast access time;
4 providing a plurality of muxes coupled to said first way in each of said banks; and
5 using the mux in a bank to remap any defective way in a bank to the first way in that same
6 bank.

1 20. The method of claim 19 further comprising the step of testing for errors in the cache.

1 21. The method of claim 19 further comprising the step of disabling a way in a bank when that
2 way is defective.

1 22. The method of claim 19 comprising a plurality of ways having a fast access time and a
2 plurality of muxes coupled to said plurality of ways in each of said banks.

1 23. The method of claim 22 wherein the plurality of muxes in a bank are used to remap any
2 defective way in a bank to a different way in that same bank.

1 24. A computer system, comprising:

2 a power supply;

3 a microprocessor comprising:

4 a set associative cache having a plurality of ways wherein the ways are segmented into a
5 plurality of banks;

6 access control logic which manages access to the cache coupled to said plurality of ways in
7 said cache;

8 a first way in said cache which has a physically shorter path to said access control logic;

9 a plurality of muxes coupled to said first way in each of said plurality of banks and coupled
10 to said access control logic; and

11 wherein the access control logic can control the mux in a bank to remap any defective way
12 in a bank to the first way in that same bank.